

TRANSMITTAL OF APPEAL BRIEF (Large Entity)Docket No.
INTL-0219-USIn Re Application Of: **SCOTT A. ROSENBERG AND ANTHONY C. MILLER**Serial No.
09/365,363Filing Date
JULY 30, 1999Examiner
N. PATELGroup Art Unit
2775Invention: **LIQUID CRYSTAL OVER SEMICONDUCTOR DISPLAY WITH ON-CHIP STORAGE**TO THE ASSISTANT COMMISSIONER FOR PATENTS:Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **AUGUST 22, 2001**The fee for filing this Appeal Brief is: **\$320.00**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re	Scott A. Rosenberg	\$	Art Unit:	2775
Applicants:	And Anthony C.	\$		
	Miller	\$		
		\$		
Serial No.:	09/365,363	\$		
		\$	Examiner:	N. Patel
Filed:	July 30, 1999	\$		
		\$		
Title:	Liquid Crystal	\$	Docket No.	INTL-0219-US
	Over Semiconductor	\$		(P7127)
	Display With On-	\$		
	Chip Storage	\$		

Commissioner for Patents
Board of Patent Appeals & Interferences
Washington, D.C. 20231

APPEAL BRIEF

Dear Sir:

Applicants respectfully appeal from the final
rejection mailed on July 18, 2001.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel
Corporation.

II. RELATED APPEALS AND INTERFERENCES

None.

III. STATUS OF THE CLAIMS

Claims 1-25 are rejected. Each rejection is appealed.

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IV. STATUS OF AMENDMENTS

The Reply to the Final Rejection mailed on August 1, 2001, was not entered by the Examiner. The Board should note that the unentered amendment sought only to cancel claims and, thus, was absolutely entitled to entry. As a result of the Examiner's inappropriate action all claims are addressed in this appeal.

V. SUMMARY OF THE INVENTION

Referring to Fig. 1, an electro-optical device 10, such as a spatial light modulator (SLM), may include a plurality of reflective mirrors 12 defined on a semiconductor substrate 14 in accordance with one embodiment of the present invention. Advantageously, the device 10 is implemented using liquid crystal over semiconductor (LCOS) technology. LCOS technology may form large screen projection displays or smaller displays (using direct view rather than projection technology). With LCOS technology, the liquid crystal display is formed in association with the same substrate that forms complementary metal oxide semiconductor (CMOS) circuit elements. The display may be a reflective liquid crystal display. See Specification at page 3, line 17 through page 4, line 4.

The device 10 may include a silicon substrate 14 with a metal layer defining the mirrors 12. The mirrors 12 may be the mirrors of an electro-optic display such as a liquid crystal display. For example, the mirrors 12 may be part of spatial light modulator (SLM) for one of the color planes of a tricolor display. Potentials applied to the mirrors 12 alter the liquid crystal to modulate the incoming light to create images which then can be directly viewed or projected onto a projection screen.

Referring to Fig. 2, each cell or pixel of the display may include a reflective mirror 24 forming one of the mirrors of one of the pixels 12 shown in Fig. 1. In one embodiment of the invention, each cell may be rectangular or square and a slight spacing may occur between each adjacent mirror 24. Thus, a rectangular array of mirrors 24 may form an array of pixel elements in conjunction with liquid crystal material 20 positioned over the mirrors 24.

The LCOS structure includes a silicon substrate 14 having doped regions 32 formed therein. The doped regions 32 may define transistors for logic elements and/or memory cells which operate in conjunction with the display pixels as will be described hereinafter. Four or more metal layers may be provided, including a metal one layer 30 which is spaced by an inter-layer dielectric (ILD) 31 from

a metal two layer 28 and a metal three layer 26. A metal four layer may form the pixel mirrors 24. Thus, for example, the metal two layer 28 may provide light blocking and the metal one layer may provide the desired interconnections for forming the semiconductor logic and memory devices. The pixel mirrors 24 may be coupled, by way of vias 32, with the other metal layers. See Specification at page 4, line 5 through page 5, line 9.

A dielectric layer 22 may be formed over the mirror 24. A liquid crystal or electro-optic material 20 is sandwiched between a pair of buffered polyimide layers 19a and 19b. One electrode of the liquid crystal device is formed by the metal layer 24. The other electrode is formed by an indium tin oxide (ITO) layer 18.

A top plate 16 may be formed of transparent material. The ITO layer 18 may be coated on the top plate 26. The polyimide layers 19a and 19b provide electrical isolation between the capacitor plates which sandwich the electro-optic material 20. However, other insulating materials may be coated on the ITO layer 18 in place of or in addition to the polyimide layers.

Using the LCOS structure, for example as depicted in Fig. 2, a memory element or array may be incorporated into the same silicon substrate which includes the pixel array.

In one embodiment of the present invention, a separate memory array 36 may be included on the same substrate 14 that includes the pixel array 42, as shown in Fig. 3. The memory array may be, for example, dynamic random access memory (DRAM). See Specification at page 5, line 10 through page 6, line 4.

The memory array 36 receives and transmits data, as indicated by the arrows on the left side of the array 36 from a display controller in a host processor-based system (not shown in Fig. 3). The array 36 also communicates with the pixel array 42 via a refresh circuit 38 utilized for both DRAM memory refresh and pixel array refresh. A digital to analog converter 40 converts the data from the memory 36 to an analog format for addressing particular pixels in the pixel array 42. Moreover, the refresh circuit 38 may feed back to the memory array 36 so that the refresh circuit 38 not only refreshes the pixels in the pixel array 42 but also refreshes the memory array 36.

Thus, in the process of rewriting the DRAM cells for their own refresh, the same refresh circuitry also updates the pixel cells. Since DRAM and pixel refresh cycles are combined into one cycle, the overall read bandwidth, sourced from the DRAM array, may be reduced. Compared to systems where two separate streams of data are

simultaneously read out of the DRAM array, less bandwidth may be used. By using only one stream for both refresh operations, combining the memory and refresh cycles into one cycle, the overall bandwidth required from the DRAM memory is reduced. See Specification at page 6, line 5 through page 7, line 2.

Referring next of Fig. 4, a processor-based host system 51 for the electro-optical device 10 includes a system memory 43 which is coupled through an interface bus 44 with a general purpose microprocessor 46 in accordance with one embodiment of the invention. The interface bus 44 also may provide processor and memory access to a media or graphics processor 48 and a display refresh controller 50. The display refresh controller is coupled by a bus 49 to the electro-optic device 10 which may be an LCOS display with integrated storage. See Specification at page 7, line 3 through page 8, line 3.

One electro-optical device 10 which may not need a periodic display refresh in some embodiments, is illustrated in Fig. 5. If the periodic display refresh is eliminated, this may also increase the available system wide bandwidth. The illustrated embodiment uses integrated memory 60 for each pixel cell 12. In some embodiments, pixel information may be passed through a digital to analog

converter (DAC) 62 to produce gray scale information. The particular manner in which pixels are arranged in the storage array and converted to analog signals may vary by implementation.

Each pixel metal electrode or top metal 12 may be coupled to a separate DAC 62. In one embodiment of the present invention, the DAC may be an eight bit DAC coupled to eight one bit storage elements 60. Each storage element 60 may, for example, be a static random access memory (SRAM) cell. Each one bit storage element 60 may be coupled by a transfer transistor 58 to a different row 56 and a column 54. Thus, the information which is used to refresh the metal mirror 12 may be stored in the memory 60. When it is desired to change the pixel information to change the displayed image, then the information in the memory 60 is refreshed. See Specification at page 8, line 4 through page 9, line 6.

Since the display refresh controller only needs to refresh new information to the display, the overall drain on the computer system including the buses and memory may be reduced, potentially yielding better performance out of the other components in the computer system which rely on these limited resources. In addition, the amount of redundant information flowing to the display may be

reduced, allowing more new information to be sent to the display. This potentially enables the display of higher resolution or higher rate images.

VI. ISSUE

- A. Is claim 13 Anticipated by Quanrud?
- B. Is Claim 14 Anticipated by Quanrud?
- C. Is Claim 17 Anticipated by Quanrud?
- D. Is Claim 1 Anticipated by Quanrud?
- E. Is Claim 9 Anticipated by Quanrud?
- F. Is Claim 21 Anticipated by Quanrud?

*Claim 13
cancelled*

VII. GROUPING OF THE CLAIMS

For convenience on appeal, claims 1-12 may be grouped; claims 14, 15, and 16 may be grouped; claims 17, 18, 19 and 20 may be grouped; and claims 1-8 may be grouped; claims 9-12 may be grouped; and claims 21-25 may be grouped.

VIII. ARGUMENT

- A. Is claim 13 anticipated by Quanrud?

Claim 13 relates to a display with a refresh circuit to refresh the memory array and the pixel array.

Claim 13 was rejected under § 102 over Quanrud '983. However, Quanrud (in column 6 cited by the Examiner) merely talks about refreshing the memory cells. It says nothing about refreshing the pixel array. Thus, there is no indication that the same refresh circuit is utilized to refresh both the memory and pixel arrays.

B. Is Claim 14 Anticipated by Quanrud?

Claim 14 modifies claim 13 and further calls for the memory array and the pixel array formed on the same semiconductor substrate with the refresh circuit.

The Examiner cites sections of the Quanrud reference indicating that the memory array and the pixel array are on the same substrate. But, none of this material says anything about where the refresh circuit is located.

Therefore, the anticipation reference with respect to claim 14 should be reversed.

C. Is Claim 17 Anticipated by Quanrud?

Quanrud fails to teach "refreshing said memory array and said pixel array in the same refresh cycle," as set forth in claim 17. In fact, none of the material cited by the Examiner in rejecting claim 17 has anything to do with

refreshing. Therefore, claim 17 and the claims dependent thereon patentably distinguish over the Quanrud reference.

D. Is Claim 1 Anticipated by Quanrud?

Claim 1 relates to a display including a liquid crystal over semiconductor (LCOS) pixel array formed in a substrate and a memory coupled to the array, the memory also formed in the substrate.

Claims 1-12 were rejected over the patent to Quanrud. However, Quanrud does not in any way relate to an LCOS structure. In Quanrud, the memory is not integrated into the same structure that also integrates the liquid crystal device. Moreover, it is not even clear that the liquid crystal device in Quanrud is, in fact, integrated into a semiconductor substrate.

For example, column 5, states that "the substrate may be any material on which the display circuit may be attached or formed. In a preferred embodiment, the substrate is a semiconductor, such as silicon, on which the display circuits are formed by one or more of a variety of methods known in the art." See column 5, lines 23-28 (emphasis added).

This language certainly does teach a liquid crystal over semiconductor device. With LCOS technology, a liquid

crystal display is formed in association with the same substrate that forms CMOS circuit elements. See the specification at p. 3, lines 25 through p. 4, line 3.

Moreover, in column 12, Quanrud states that the pixels may be liquid crystal displays, spatial light modulators, gratings, mirror light valves, and LED displays. Certainly, the variety of technologies amenable to Quanrud's display indicates that, in fact, Quanrud is not talking about LCOS technology. Moreover, the fact that nowhere does Quanrud ever mention LCOS technology further adds force to this conclusion.

In short, there is nothing in Quanrud that suggests a liquid crystal over semiconductor pixel array, or a memory formed in the same structure with the pixel array. Therefore, claim 1 is in condition for allowance.

E. Is Claim 9 Anticipated by Quanrud?

Similarly, method claim 9 calls for forming pixel array in a liquid crystal over semiconductor substrate. A memory is formed in the liquid crystal over semiconductor substrate. Again, no such method steps are anywhere suggested in Quanrud. Therefore, claim 9 is patentably distinguishable over Quanrud.

F. Is Claim 21 Anticipated by Quanrud?

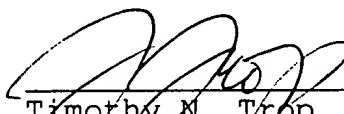
Finally, claim 21 calls for a display with an LCOS substrate that also includes a memory array. As discussed above, Quanrud fails to teach such a structure and therefore the claims patentably distinguish over Quanrud.

XI. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: 10/10/01



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APPENDIX OF CLAIMS

The claims on appeal are:

- 1 1. A display comprising:
2 a semiconductor substrate;
3 a liquid crystal over semiconductor pixel array
4 formed in said substrate; and
5 a memory coupled to said array, said memory also
6 formed in said substrate.

- 1 2. The display of claim 1 wherein said pixel array
2 includes a plurality of pixels each including a memory
3 cell.

- 1 3. The display of claim 2 wherein said memory cells
2 are static random access memory cells.

- 1 4. The display of claim 1 wherein said pixel array
2 is coupled to said memory by a digital to analog converter.

- 1 5. The display of claim 1 wherein said memory
2 includes a cell associated with each of a plurality of
3 pixels of the pixel array.

- 1 6. The display of claim 1 wherein said pixel array
2 forms a reflective liquid crystal spatial light modulator.

1 7. The display of claim 1 wherein said memory a
2 dynamic random access memory, and said display includes a
3 refresh circuit, said refresh circuit adapted to refresh
4 both said dynamic random access memory and said pixel
5 array.

1 8. The display of claim 1 wherein said pixel array
2 is adapted to eliminate the need for a periodic pixel
3 refresh cycle.

1 9. A method for displaying information comprising:
2 forming a pixel array in a liquid crystal over
3 semiconductor substrate; and
4 forming a memory in said liquid crystal over
5 semiconductor substrate, with said memory coupled to said
6 pixel array.

1 10. The method of claim 9 wherein forming a memory
2 includes forming a memory associated with each pixel of
3 said pixel array.

1 11. The method of claim 9 wherein forming a memory
2 includes forming a volatile memory and refreshing said
3 volatile memory and said pixel array in the same refresh
4 cycle.

1 12. The method of claim 9 including displaying
2 information without using a periodic refresh cycle.

1 13. A display comprising:
2 a memory array;
3 a pixel array; and
4 a refresh circuit coupled to said memory array
5 and said pixel array, said refresh circuit adapted to
6 refresh said memory array and said pixel array.

1 14. The display of claim 13 wherein said memory array
2 and said pixel array are formed in the same semiconductor
3 substrate with said refresh circuit.

1 15. The display of claim 14 wherein said substrate is
2 a liquid crystal over semiconductor substrate, said pixel
3 array including a plurality of electrodes adapted to
4 interact with a liquid crystal material over said pixel
5 array.

1 16. The display of claim 13 wherein said memory array
2 is formed of dynamic random access memory.

1 17. A method for displaying information comprising:
2 providing a pixel array in a semiconductor
3 substrate;
4 providing a memory array in said substrate; and
5 refreshing said memory array and said pixel array
6 in the same refresh cycle.

1 18. The method of claim 17 including forming said
2 memory and pixel arrays in a liquid crystal over
3 semiconductor substrate.

1 19. The method of claim 17 including storing pixel
2 data in said memory array.

1 20. The method of claim 17 including providing a
2 liquid crystal material over said pixel array.

1 21. A processor-based system comprising:
2 a processor;
3 an interface bus coupled to said processor; and
4 a display coupled to said processor, said display
5 including a liquid crystal over semiconductor substrate,
6 said substrate including a memory array and a pixel array
7 coupled to said memory array.

1 22. The system of claim 21 wherein said memory array
2 includes a plurality of cells, each cell coupled to a pixel
3 of said pixel array.

1 23. The system of claim 22 wherein said memory cells
2 are static random access memory cells.

1 24. The system of claim 23 wherein said pixel array
2 is a reflective liquid crystal array.

1 25. The system of claim 24, said memory including a
2 plurality of storage locations at each pixel and a digital
3 to analog converter coupling each of said storage locations
4 to a different pixel cell.